

Plug-in Signal Conditioners M-UNIT

A/D CONVERTER

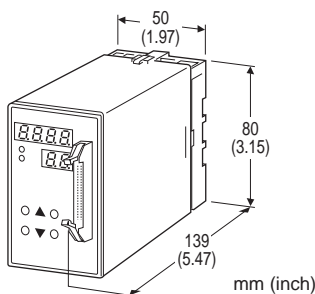
(16-bit resolution)

Functions & Features

- Converts a DC input into parallel digital signals with parity check
- BCD, binary, reflected binary, two's complement outputs selectable
- Open collector or CMOS for output levels
- Output can be scaled and displayed in convenient engineering unit
- Loop test output
- Response time adjustable within 0.15 and 60 sec.

Typical Applications

- Interface of analog signal to computers and PLC
- Input to a digital panel meter



MODEL: AD3V-[1][2]-[3][4]

ORDERING INFORMATION

- Code number: AD3V-[1][2]-[3][4]
- Specify a code from below for each [1] through [4].
(e.g. AD3V-S1C-M2/Q)
- Specify the specification for option code /Q
(e.g. /C01/S01)

[1] INPUT

Current

Z1: Range 0 - 50 mA DC (Input resistance 100 Ω)

Voltage

S1: Range -1 - + 1 V DC (Input resistance 100 kΩ min.)

S2: Range -10 - +10 V DC (Input resistance 1 MΩ min.)

S3: Range -30 - +30 V DC (Input resistance 1 MΩ min.)

[2] OUTPUT LEVEL

A: Open collector (NPN)

B: Open collector (PNP)

C: CMOS level

[3] POWER INPUT

AC Power

M2: 100 - 240 V AC (Operational voltage range 85 - 264 V, 47 - 66 Hz)

DC Power

R3: 12 - 24 V DC

(Operational voltage range 10.8 - 26.4 V, ripple 10 %p-p max.)

P: 110 V DC

(Operational voltage range 85 - 150 V, ripple 10 %p-p max.)

[4] OPTIONS

blank: none

/Q: With options (specify the specification)

SPECIFICATIONS OF OPTION: Q (multiple selections)

COATING (For the detail, refer to M-System's web site.)

/C01: Silicone coating

/C02: Polyurethane coating

/C03: Rubber coating

TERMINAL SCREW MATERIAL

/S01: Stainless steel

RELATED PRODUCTS

- Connector terminal block (model: CNT)
- Special cable (model: MCN26)

GENERAL SPECIFICATIONS

Construction: Plug-in

Connection

Input & power: M3.5 screw terminals

Output: 26-pin connector (OMRON XG4A-2634)

Paired connector: OMRON XG4M-2630-T, XG5M-263x-N

Cover: OMRON XG5S-2612

Screw terminal: Chromated steel (standard) or stainless steel

Housing material: Flame-resistant resin (black)

Isolation: Input to output to power

Zero adjustment: -99.99 - 99.99 % (front)

Span adjustment: -99.99 - 99.99 % (front)

Setting: (Front key pad)

- Scaled range
- Moving average
- Output code
- Available number of bits
- POL/OVF output logic
- Data output logic
- HOLD input logic
- DAV output logic
- DAV output time
- Output rate 'n' ratio



- Parity check
- etc.

For detailed information, refer to the instruction manual.

■ DISPLAY

LED: 7 mm (.28") 7 segment, red

Number of display digits: 4 digits for DATA display; 2 digits for ITEM display

PV indication: Output signal in engineering unit

Overrange indication: LEDs blinking

Power saving mode: Displays turn off if the keys are untouched for a preset time period

PL1 (POL) LED: Red light turns on at negative polarity.

PL2 (HOLD) LED: Red light turns on at HOLD.

INPUT SPECIFICATIONS

■ **DC Current:** 0 - 50 mA DC; shunt resistor attached to input terminals (0.5 W)

Operational range: 0 - 70 mA DC (with 100 Ω/0.5 W)

Usable range:

- Max. range: 0 - 50 mA DC
- Min. step: 0.1 mA DC

Factory default: 4 - 20 mA DC

- Input setting must: 100 % setting \geq 0 % setting
- Input value is operational range or 15 to +115 %.

■ DC Voltage

Operation range:

S1: -1.15 to +1.15 V DC

S2: -11.5 to +11.5 V DC

S3: -34.5 to +34.5 V DC

Usable range:

- Max. range:

S1: -1 to +1 V DC

S2: -10 to +10 V DC

S3: -30 to +30 V DC

- Min. step:

S1: 10m V DC

S2: 100m V DC

S3: 100m V DC

Factory default:

S1: -1 to +1 V DC

S2: -10 to +10 V DC

S3: -30 to +30 V DC

- Input setting must: 100 % setting \geq 0 % setting
- Input value is operational range or 15 to +115 %.

■ **Hold Input:** TTL level (5 V - CMOS level)

Commands to stop data renewal;

Choose from below:

Hold with low or short

Hold with high or open

(Default Setting will be hold with low or short)

OUTPUT SPECIFICATIONS

■ **Output Code:** Code, logic and scaling are user-selectable.

BCD with polarity

Binary with polarity

Offset binary

Two's complement

Reflected binary

■ **Output Level**

- **Open Collector**

Max. collector-emitter voltage: 30 V DC

Max. collector current: 30 mA

Saturation voltage:

NPN \leq 1.1 V negative common

PNP \leq 2.0 V positive common

- **CMOS Level**

H output: \geq 4.5 V DC

L output: \leq 0.5 V DC

Common: Negative

■ **POL output (Polarity):** Same logic and level as for the output code; logic user-selectable

■ **OVF output (Overflow):** Same logic and level as for the output code; logic user-selectable

■ **DAV output (Data available):** Same level as for the output code; logic user-selectable

INSTALLATION

Power consumption

- **AC:** Approx. 10 VA

- **DC:** Approx. 4 W (160 mA at 24 V)

Operating temperature: -5 to +55°C (23 to 131°F)

Operating humidity: 30 to 90 %RH (non-condensing)

Mounting: Surface or DIN rail

Weight: 260 g (0.57 lb)

PERFORMANCE in percentage of span

Accuracy: ± 0.1 %

Temp. coefficient: ± 0.015 %/°C (± 0.008 %/°F)

Resolution: 16 bits

Response time: 0.15 - 60 sec. (0 - 90 %) programmable at front key pad.

Line voltage effect: ± 0.1 % over voltage range

Insulation resistance: \geq 100 MΩ with 500 V DC

Dielectric strength: 2000 V AC @1 minute (input to output to power to ground)

STANDARDS & APPROVALS

CE conformity:

EMC Directive (2004/108/EC)

EMI EN 61000-6-4: 2007

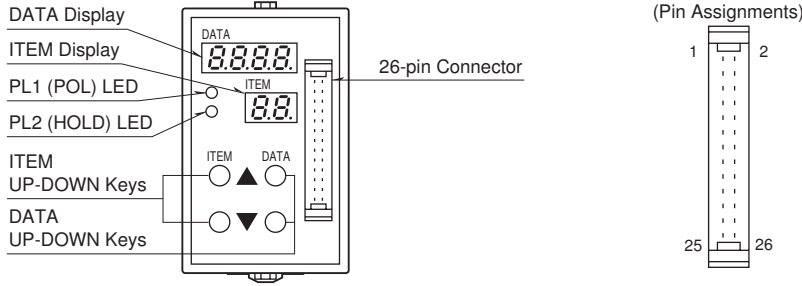
EMS EN 61000-6-2: 2005

Low Voltage Directive (2006/95/EC)

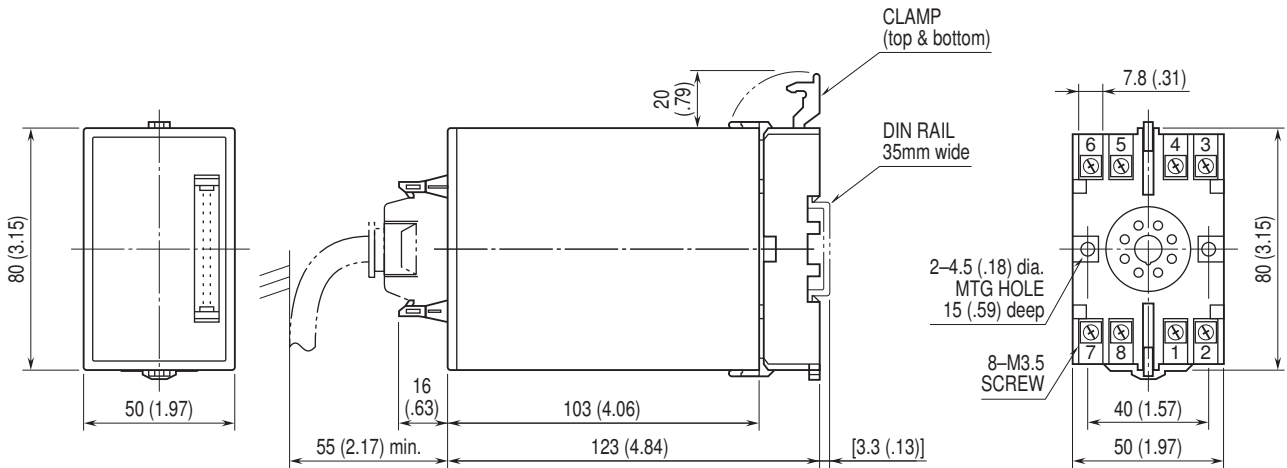


EN 61010-1: 2001
 Installation Category II
 Pollution Degree 2
 Input or output to power: Reinforced insulation (300 V)
 Input to output: Basic insulation (300 V)

EXTERNAL VIEW

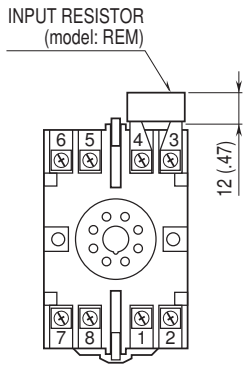


DIMENSIONS unit: mm (inch)



•When mounting, no extra space is needed between units.

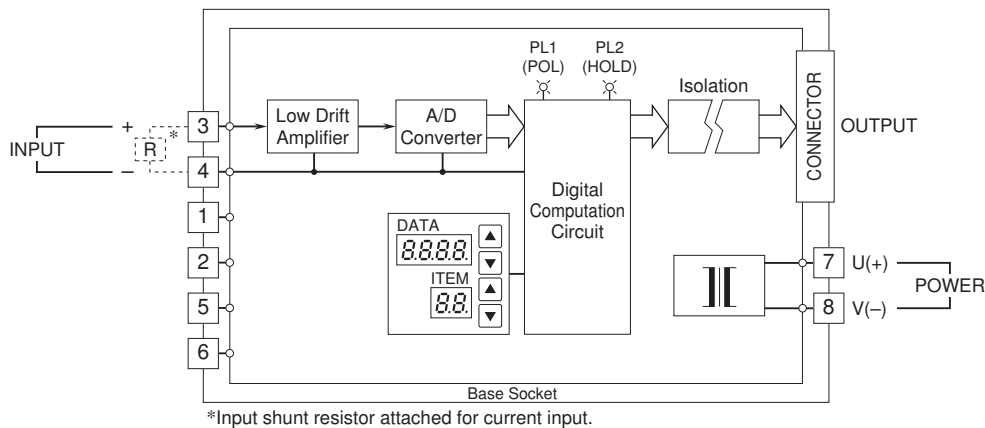
TERMINAL ASSIGNMENTS unit: mm (inch)



Input shunt resistor attached for current input.

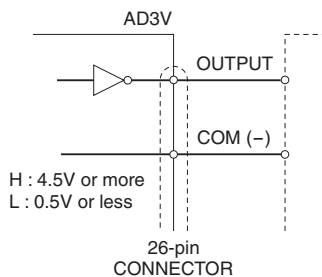


SCHEMATIC CIRCUITRY & CONNECTION DIAGRAM

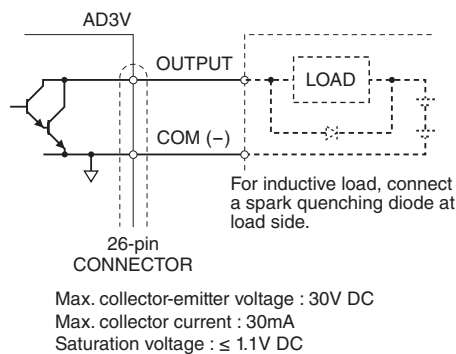


■ Connection Examples

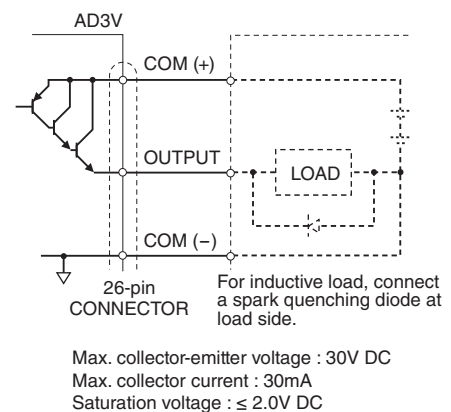
• CMOS LEVEL (5V-CMOS)



• OPEN COLLECTOR (NPN)



• OPEN COLLECTOR (PNP)



OUTPUT CONNECTOR (26 pins)

• BCD OUTPUT

PIN NO.	ASSIGNMENT	PIN NO.	ASSIGNMENT
1	1 10^0	17	COM ^{*1}
2	2 10^0	18	COM (-)
3	4 10^0	19	OVF
4	8 10^0	20	POL
5	1 10^1	21	DAV
6	2 10^1	22	HOLD ^{*2}
7	4 10^1	23	P ⁰ ^{*3}
8	8 10^1	24	P ¹
9	1 10^2	25	P ²
10	2 10^2	26	P ³
11	4 10^2		
12	8 10^2		
13	1 10^3		
14	2 10^3		
15	4 10^3		
16	8 10^3		

• BINARY, TWO'S COMPLEMENT OUTPUTS

PIN NO.	ASSIGNMENT	PIN NO.	ASSIGNMENT
1	B ⁰	17	COM ^{*1}
2	B ¹	18	COM (-)
3	B ²	19	OVF
4	B ³	20	POL
5	B ⁴	21	DAV
6	B ⁵	22	HOLD ^{*2}
7	B ⁶	23	P ⁰ ^{*4}
8	B ⁷	24	P ¹
9	B ⁸	25	P ²
10	B ⁹	26	P ³
11	B ¹⁰		
12	B ¹¹		
13	B ¹²		
14	B ¹³		
15	B ¹⁴		
16	B ¹⁵		

*1. For open collector (NPN) and CMOS level, COM (-). For open collector(PNP), COM (+).

*2. HOLD signal is for input, the others are for output.

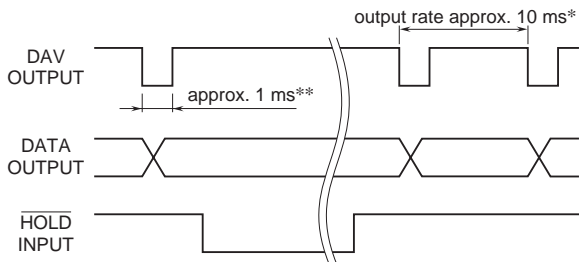
*3. P⁰ corresponds to $\times 10^0$, P¹ to $\times 10^1$, P² to $\times 10^2$, P³ to $n \times 10^3$.

*4. P⁰ corresponds to B⁰ through B³, P¹ to B⁴ through B⁷, P² to B⁸ through B¹¹, P³ to B¹² through B¹⁵.

Note: With the number of bits set to 14 (or 12, 10, 8) with ITEM 10, Pin No. 1 - 14 (or 1 - 12, 1 - 10, 1 - 8) are valid.



TIMING CHART



Data output is halt during $\overline{\text{HOLD}}$ input.

DAV is output during DATA output.

* Varies by individual module. Set to 'n' times with ITEM 20.

**Selectable with ITEM 17.

INPUT-OUTPUT RELATION EXAMPLES

*FS

-FS stands for -15 % of the input range, which is configured by ITEM22, 0 % input voltage and ITEM23, 100 % input voltage.

+FS stands for +115 % of the input range.

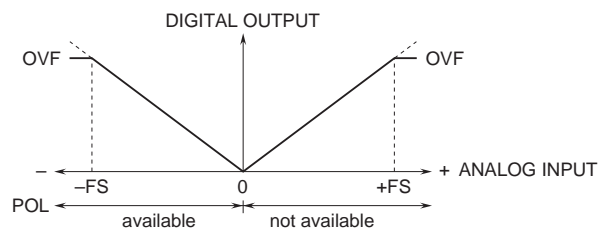
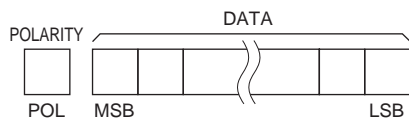
*OVF

When one of the following conditions is true, the digital output overflows (OVF).

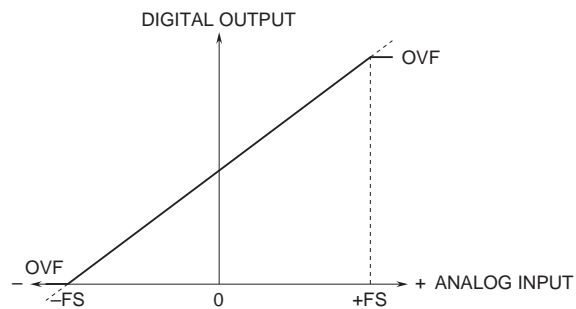
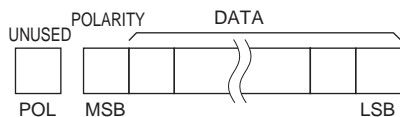
- 1) When the input signal is out of the range between -FS and +FS.
- 2) When the display value (= output signal) exceeds the display range.

The display range differs according to output code. For example, in case of BCD with polarity, it is -9999 to 9999. Please refer to the instruction manual for detail.

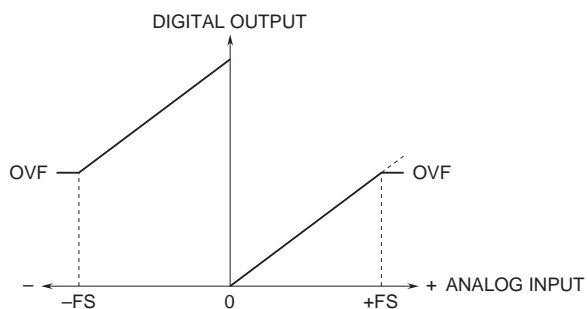
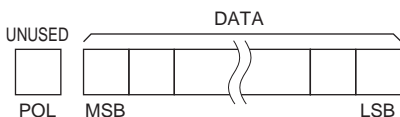
■BCD, BINARY (WITH POLARITY)



■OFFSET BINARY



■TWO'S COMPLEMENT



OUTPUT DATA & PARITY BIT RELATIONSHIP

Hi and Lo indicate the voltage level. Parity logic is unchanged. (ITEM 12 = I12; ITEM 14 = I14)

■ OPEN COLLECTOR (NPN)

• Positive Logic I14 : 1, Lo : False, Hi: True

DATA	8	4	2	1	PARITY	
					Even I12 : 0	Odd I12 : 1
0	Lo	Lo	Lo	Lo	Lo	Hi
1	Lo	Lo	Lo	Hi	Hi	Lo
2	Lo	Lo	Hi	Lo	Hi	Lo
3	Lo	Lo	Hi	Hi	Lo	Hi
4	Lo	Hi	Lo	Lo	Hi	Lo
5	Lo	Hi	Lo	Hi	Lo	Hi
6	Lo	Hi	Hi	Lo	Lo	Hi
7	Lo	Hi	Hi	Hi	Hi	Lo
8	Hi	Lo	Lo	Lo	Hi	Lo
9	Hi	Lo	Lo	Hi	Lo	Hi
10	Hi	Lo	Hi	Lo	Lo	Hi
11	Hi	Lo	Hi	Hi	Hi	Lo
12	Hi	Hi	Lo	Lo	Lo	Hi
13	Hi	Hi	Lo	Hi	Hi	Lo
14	Hi	Hi	Hi	Lo	Hi	Lo
15	Hi	Hi	Hi	Hi	Lo	Hi

■ CMOS, OPEN COLLECTOR (PNP)

• Positive Logic I14 : 0, Lo : False, Hi: True

DATA	8	4	2	1	PARITY	
					Odd I12 : 0	Even I12 : 1
0	Lo	Lo	Lo	Lo	Hi	Lo
1	Lo	Lo	Lo	Hi	Lo	Hi
2	Lo	Lo	Hi	Lo	Lo	Hi
3	Lo	Lo	Hi	Hi	Hi	Lo
4	Lo	Hi	Lo	Lo	Lo	Hi
5	Lo	Hi	Lo	Hi	Hi	Lo
6	Lo	Hi	Hi	Lo	Hi	Lo
7	Lo	Hi	Hi	Hi	Lo	Hi
8	Hi	Lo	Lo	Lo	Lo	Hi
9	Hi	Lo	Lo	Hi	Hi	Lo
10	Hi	Lo	Hi	Lo	Hi	Lo
11	Hi	Lo	Hi	Hi	Lo	Hi
12	Hi	Hi	Lo	Lo	Hi	Lo
13	Hi	Hi	Lo	Hi	Lo	Hi
14	Hi	Hi	Hi	Lo	Lo	Hi
15	Hi	Hi	Hi	Hi	Hi	Lo

• Negative Logic I14 : 0, Lo : True, Hi: False

DATA	8	4	2	1	PARITY	
					Even I12 : 0	Odd I12 : 1
0	Hi	Hi	Hi	Hi	Lo	Hi
1	Hi	Hi	Hi	Lo	Hi	Lo
2	Hi	Hi	Lo	Hi	Hi	Lo
3	Hi	Hi	Lo	Lo	Lo	Hi
4	Hi	Lo	Hi	Hi	Hi	Lo
5	Hi	Lo	Hi	Lo	Lo	Hi
6	Hi	Lo	Lo	Hi	Lo	Hi
7	Hi	Lo	Lo	Lo	Hi	Lo
8	Lo	Hi	Hi	Hi	Hi	Lo
9	Lo	Hi	Hi	Lo	Lo	Hi
10	Lo	Hi	Lo	Hi	Lo	Hi
11	Lo	Hi	Lo	Lo	Hi	Lo
12	Lo	Lo	Hi	Hi	Lo	Hi
13	Lo	Lo	Hi	Lo	Hi	Lo
14	Lo	Lo	Lo	Hi	Hi	Lo
15	Lo	Lo	Lo	Lo	Lo	Hi

• Negative Logic I14 : 1, Lo : True, Hi: False

DATA	8	4	2	1	PARITY	
					Odd I12 : 0	Even I12 : 1
0	Hi	Hi	Hi	Hi	Hi	Lo
1	Hi	Hi	Hi	Lo	Lo	Hi
2	Hi	Hi	Lo	Hi	Lo	Hi
3	Hi	Hi	Lo	Lo	Hi	Lo
4	Hi	Lo	Hi	Hi	Lo	Hi
5	Hi	Lo	Hi	Lo	Hi	Lo
6	Hi	Lo	Lo	Hi	Hi	Lo
7	Hi	Lo	Lo	Lo	Lo	Hi
8	Lo	Hi	Hi	Hi	Lo	Hi
9	Lo	Hi	Hi	Lo	Hi	Lo
10	Lo	Hi	Lo	Hi	Hi	Lo
11	Lo	Hi	Lo	Lo	Lo	Hi
12	Lo	Lo	Hi	Hi	Hi	Lo
13	Lo	Lo	Hi	Lo	Lo	Hi
14	Lo	Lo	Lo	Hi	Lo	Hi
15	Lo	Lo	Lo	Lo	Hi	Lo



Specifications are subject to change without notice.

